## 8085 Microprocessor Pin Configuration

The 40 pins of[the microprocessor](https://www.elprocus.com/know-about-architecture-of-the-intel-8080-microprocessor/) can be divided into six groups such as address bus, data bus, control signals & status signals; power supply & frequency, externally started signals and serial input/output ports.

8085 Microprocessor pin Configuration

**Address Bus (A8-A15)**

The address bus pins are ranges from A8 to A15 and these are mainly applicable to the most considerable memory address bit.

**Address Bus (or) Data Bus (AD0-AD7)**

The address bus pins or data bus pins are ranges from AD0 to AD7, and these pins are applicable for LSB (least significant bits) of the address bus in the primary apparatus CLK cycle as well as employed as a data bus for second clock cycle & third clock cycle.  
A CLK cycle can be designed as, the time in use among two oscillator’s nearby pulses, or simply it can refer to zero volts. Here the first clock is the primary transition of pulse ranges from 0V to 5V & then reaches back to 0V.

**Address Latch Enable (ALE)**

Basically, ALE assists in de-multiplexing the data bus as well as low order address. This will go high throughout the primary clock cycle as well as allows the address bits with low order. The address bus with low order is added for memory otherwise any exterior latch.

**Status Signal (IO/M)**

The status signal IO/M resolves whether the address is intended for memory or input/output. When the address is high then the address of the address bus is used for the devices of input/output devices. When the address is low then the address of the address bus is used for the memory.

**Status Signals (S0-S1)**

The status signals S0, S1 gives different functions as well as status based on their status.

* When the S0, S1 are 01 then the operation will be HALT.
* the S0, S1 is 10 then the operation will be WRITE
* When the S0, S1 is 10 then the operation will be READ
* When the S0, S1 are 11 then the operation will be FETCH

**Active Low Signal (RD)**

The RD is an energetic low signal and an operation is executed whenever the indication goes small, and it is used for controlling the microprocessor READ operation. When RD pin goes small then the 8085 microprocessor understands the information from I/O device or memory.

**Active Low Signal (WR)**

This is an energetic low signal, and it controls the microprocessor’s write operations. Whenever WR pin goes small, then the information will be written to the I/O device or memory.

**READY**

The READY pin is employed with the 8085 microprocessor for ensuring whether a device is set for accepting or transferring data. A device may be an A/D converter or LCD display, etc. These devices are associated with the 8085 microprocessor with the READY-pin. When this pin is high, the device is prepared for transferring the information, if it is not then the microprocessor stays until this pin goes high.

**HOLD**

The HOLD pin specifies when any device is demanding the employ of address as well as a data bus. The two devices are LCD as well as A/D converter. Assume that if [A/D converter](https://www.elprocus.com/analog-to-digital-converter/) is employing the address bus as well as a data bus. When LCD desires the utilize of both the buses by providing HOLD signal, subsequently the microprocessor transmits the control signal toward the LCD after that the existing cycle will be ended. When [the LCD](https://www.elprocus.com/difference-alphanumeric-display-and-customized-lcd/) procedure is over, then the control signal is transmitted reverse to A/D converter.

**HLDA**

This is the response signal of HOLD, and it specifies whether this signal is obtained or not obtained. After the implementation of HOLD demand, this signal will go low.

**INTR**

This is an interrupt signal, and the priority of this among[the interrupts](https://www.elprocus.com/types-of-interrupts-in-8051-microcontroller-and-interrupt-programming/) is low. This signal can be allowed or not allowed by the software. When INTR pin goes high then the 8085 microprocessor completes the instruction of current which is being executed and then recognizes the INTR signal and progresses it.

**INTA**

When the 8085 microprocessor gets an interrupt signal, then it should be recognized. This will be done by INTA. As a result, when the interrupt will be obtained then INTA will go high.

**RST 5.5, RST 6.5, RST 7.5**

These pins are the restart maskable interrupts or **Vectored Interrupts**, used to insert an inner restart function repeatedly. All these interrupts are maskable, they can be allowed or not allowed by using programs.

**TRAP**

Along with the 8085 microprocessor interrupts, TRAP is a**non-maskable interrupt**, and it doesn’t allow or stopped by a program. TRAP has the maximum precedence between the interrupts. The priority order from maximum to low includes TRAP, RST 5.5, RST 6.5, RST 7.5, and INTR.

**RESET IN**

RESET IN pin is used to reset the program counter toward zero and rearranges interrupt enable as well as HLDA [flip-flops](https://www.elprocus.com/digital-electronics-flip-flop-circuit-types-and-applications/) (FFs). The central processing unit is detained in RST condition till this pin is high. But the registers as well as flags won’t get damaged apart from instruction register.

**RST (RESET) OUT**

RESET OUT pin specifies that the central processing unit has been rearranged with RST IN.

**X1 X2**

X1, X2 terminals that are associated with the exterior oscillator for generating the required as well as appropriate operation of a clock.

**CLK**

Sometimes it is compulsory to generate CLK o/PS from 8085 microprocessors so they can be used in favor of other peripherals or else other digital integrated circuits. This is offered with CLK pin. Its frequency is continually similar because the frequency at which the microprocessor works.

**SID**

This is a serial i/p data, and the information on this pin is uploaded into the 7th-bit of the accumulator while RIM (Read Interrupt Mask) instruction is performed. RIM verifies the interrupt whether it is covered or not covered.

**SOD**

This is the serial o/p data, and the data on this pin sends its output toward the 7th-bit of the accumulator whenever an instruction of SIM is performed.

**VSS and VCC**

VSS is a ground pin whereas Vcc is +5v pin. Therefore the **8085 pin diagram**, as well as signals, are discussed in detail.

Thus, this is all about [the 8085 microprocessor](https://en.wikipedia.org/wiki/Intel_8085). From the above information finally, we can conclude that the actual name of this processor is 8085A.

CONCLUSION:

From this experiment we have came to know the use of 8085 microprocessor . Also how the microprocessor works and instruction of 8085. And execution of 8085 microprocessor.

## 8086 Microprocessor Pin Configuration

Let us now discuss the signals in detail −

**Power supply and frequency signals**

It uses 5V DC supply at VCC pin 40, and uses ground at VSS pin 1 and 20 for its operation.

**Clock signal**

Clock signal is provided through Pin-19. It provides timing to the processor for operations. Its frequency is different for different versions, i.e. 5MHz, 8MHz and 10MHz.

**Address/data bus**

AD0-AD15. These are 16 address/data bus. AD0-AD7 carries low order byte data and AD8AD15 carries higher order byte data. During the first clock cycle, it carries 16-bit address and after that it carries 16-bit data.

**Address/status bus**

A16-A19/S3-S6. These are the 4 address/status buses. During the first clock cycle, it carries 4-bit address and later it carries status signals.

**S7/BHE**

BHE stands for Bus High Enable. It is available at pin 34 and used to indicate the transfer of data using data bus D8-D15. This signal is low during the first clock cycle, thereafter it is active.

**Read(*$\overline{RD}$*)**

It is available at pin 32 and is used to read signal for Read operation.

**Ready**

It is available at pin 22. It is an acknowledgement signal from I/O devices that data is transferred. It is an active high signal. When it is high, it indicates that the device is ready to transfer data. When it is low, it indicates wait state.

**RESET**

It is available at pin 21 and is used to restart the execution. It causes the processor to immediately terminate its present activity. This signal is active high for the first 4 clock cycles to RESET the microprocessor.

**INTR**

It is available at pin 18. It is an interrupt request signal, which is sampled during the last clock cycle of each instruction to determine if the processor considered this as an interrupt or not.

**NMI**

It stands for non-maskable interrupt and is available at pin 17. It is an edge triggered input, which causes an interrupt request to the microprocessor.

$\overline{TEST}$

This signal is like wait state and is available at pin 23. When this signal is high, then the processor has to wait for IDLE state, else the execution continues.

**MN/*$\overline{MX}$***

It stands for Minimum/Maximum and is available at pin 33. It indicates what mode the processor is to operate in; when it is high, it works in the minimum mode and vice-aversa.

**INTA**

It is an interrupt acknowledgement signal and id available at pin 24. When the microprocessor receives this signal, it acknowledges the interrupt.

**ALE**

It stands for address enable latch and is available at pin 25. A positive pulse is generated each time the processor begins any operation. This signal indicates the availability of a valid address on the address/data lines.

**DEN**

It stands for Data Enable and is available at pin 26. It is used to enable Transreceiver 8286. The transreceiver is a device used to separate data from the address/data bus.

**DT/R**

It stands for Data Transmit/Receive signal and is available at pin 27. It decides the direction of data flow through the transreceiver. When it is high, data is transmitted out and vice-a-versa.

**M/IO**

This signal is used to distinguish between memory and I/O operations. When it is high, it indicates I/O operation and when it is low indicates the memory operation. It is available at pin 28.

**WR**

It stands for write signal and is available at pin 29. It is used to write the data into the memory or the output device depending on the status of M/IO signal.

**HLDA**

It stands for Hold Acknowledgement signal and is available at pin 30. This signal acknowledges the HOLD signal.

**HOLD**

This signal indicates to the processor that external devices are requesting to access the address/data buses. It is available at pin 31.

**QS1 and QS0**

These are queue status signals and are available at pin 24 and 25. These signals provide the status of instruction queue. Their conditions are shown in the following table −

|  |  |  |
| --- | --- | --- |
| **QS0** | **QS1** | **Status** |
| 0 | 0 | No operation |
| 0 | 1 | First byte of opcode from the queue |
| 1 | 0 | Empty the queue |
| 1 | 1 | Subsequent byte from the queue |

**S0, S1, S2**

These are the status signals that provide the status of operation, which is used by the Bus Controller 8288 to generate memory & I/O control signals. These are available at pin 26, 27, and 28. Following is the table showing their status −

|  |  |  |  |
| --- | --- | --- | --- |
| **S2** | **S1** | **S0** | **Status** |
| 0 | 0 | 0 | Interrupt acknowledgement |
| 0 | 0 | 1 | I/O Read |
| 0 | 1 | 0 | I/O Write |
| 0 | 1 | 1 | Halt |
| 1 | 0 | 0 | Opcode fetch |
| 1 | 0 | 1 | Memory read |
| 1 | 1 | 0 | Memory write |
| 1 | 1 | 1 | Passive |

**LOCK**

When this signal is active, it indicates to the other processors not to ask the CPU to leave the system bus. It is activated using the LOCK prefix on any instruction and is available at pin 29.

**RQ/GT1 and RQ/GT0**

These are the Request/Grant signals used by the other processors requesting the CPU to release the system bus. When the signal is received by CPU, then it sends acknowledgment. RQ/GT0 has a higher priority than RQ/GT1.

**CONCLUSION:**

From this experiment we have come to know that 8086 microprocessor is an enhanced version of 8085 microprocessor. It is a 16bit microprocessor having 20 address line and 16 data lines.